IN THE CLAIMS

1-18. (Previously Canceled)

19. (Previously Amended) A dynamic random access memory (DRAM), comprising:

an array of memory cells formed on an integrated circuit substrate; and

a substrate voltage regulator circuit coupled to the integrated circuit substrate for setting a substrate voltage bias level, including:

a series of diodes coupled between a supply voltage source and the substrate, and at least one bypass transistor coupled to at least one diode in the series of diodes for electrically bypassing at least one diode.

20. (Previously Amended) The DRAM of claim 19, wherein the substrate voltage regulator circuit comprises:

a series of diode connected transistors coupled between a supply voltage source and the integrated circuit substrate, and at least one bypass transistor coupled to at least one diode connected transistor in the series of diode connected transistors for electrically bypassing the one diode connected transistor.

21. (Previously Added) The DRAM of claim 19, wherein each diode of the series of diodes has a junction voltage drop, and the substrate voltage bias level is defined by a supply voltage level minus junction voltage drops of unbypassed diodes of the series of diodes.

22. (Previously Added) A dynamic random access memory (DRAM), comprising:

an array of memory cells formed on a substrate;

a number of wordlines and a number of bitlines coupled to the array of memory cells;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level;

wherein the substrate voltage regulator circuit comprises a series of diodes coupled between a supply voltage source and the substrate; and

wherein the substrate voltage regulator circuit comprises at least one bypass transistor coupled to at least one diode in the series of diodes for electrically bypassing at least one diode.

23. (Previously Added) The DRAM of claim 22 wherein the substrate voltage regulator circuit includes a plurality of bypass transistors, each one of the plurality of bypass transistors coupled to at least one diode in the series of diodes for electrically bypassing a plurality of diodes.

24. (Previously Added) The DRAM of claim 22 wherein at least one bypass transistor is coupled to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

25. (Previously Added) The DRAM of claim 22 wherein the at least one bypass transistor is turned off during normal operation of the integrated circuit such that at least one diode is unbypassed during normal operation but can be selectively bypassed during testing operations.

26. (Previously Added) The DRAM of claim 22 wherein the at least one bypass transistor is turned on during normal operation of the integrated circuit such that at least one diode is bypassed during normal operation but can be selectively unbypassed during testing operations.

27. (Previously Added) A dynamic random access memory (DRAM), comprising:

an array of memory cells formed on a substrate;

a number of wordlines and a number of bitlines coupled to the array of memory cells;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level;

wherein the substrate voltage regulator circuit comprises a series of diodes coupled between a supply voltage source and the substrate; and

wherein the substrate voltage regulator circuit comprises at least one bypass transistor coupled to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

28. (Previously Added) The DRAM of claim 27 wherein the at least one bypass transistor is turned off during normal operation of the integrated circuit such that at least one diode is unbypassed during normal operation but can be selectively bypassed during testing operations.

29. (Previously Added) The DRAM of claim 27 wherein the at least one bypass transistor is turned on during normal operation of the integrated circuit such that at least one diode is bypassed during normal operation but can be selectively unbypassed during testing operations.

30. (Previously Added) A dynamic random access memory (DRAM), comprising:

an array of memory cells formed on a substrate;

a number of wordlines and a number of bitlines coupled to the array of memory cells;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level;

wherein the substrate voltage regulator circuit comprises a series of diodes coupled between a supply voltage source and the substrate; and

wherein the substrate voltage regulator circuit comprises a plurality of bypass transistors coupled to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

31. (Previously Added) The DRAM of claim 30 wherein the at least one bypass transistor is turned off during normal operation of the integrated circuit such that at least one diode is unbypassed during normal operation but can be selectively bypassed during testing operations.

32. (Previously Added) The DRAM of claim 30 wherein the at least one bypass transistor is turned on during normal operation of the integrated circuit such that at least one diode is bypassed during normal operation but can be selectively unbypassed during testing operations.

33. (Previously Added) A dynamic random access memory (DRAM), comprising:

an array of memory cells formed on a substrate;

a number of wordlines and a number of bitlines coupled to the array of memory cells;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level, the substrate voltage regulator circuit comprising a series of diode connected transistors coupled between a supply voltage source and the substrate, and at least one bypass transistor coupled to at least one diode connected transistor in the series of diode connected transistors for electrically bypassing at least one diode connected transistor,

each diode connected transistor of the series of diode connected transistors has a junction voltage drop, and the substrate voltage bias level is defined by a supply voltage level minus junction voltage drops of unbypassed diode connected transistors of the series of diode connected transistors.

34. (Previously Added) The DRAM of claim 33 wherein the at least one bypass transistor is coupled to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors.

35. (Previously Added) The DRAM of claim 33 wherein the at least one bypass transistor is turned off during normal operation of the integrated circuit such that at least one diode is unbypassed during normal operation but can be selectively bypassed during testing operations.

36. (Previously Added) The DRAM of claim 33 wherein the at least one bypass transistor is turned on during normal operation of the integrated circuit such that at least one diode is bypassed during normal operation but can be selectively unbypassed during testing operations.

37. (Previously Added) A dynamic random access memory (DRAM), comprising:

an array of memory cells formed on a substrate;

a number of wordlines and a number of bitlines coupled to the array of memory cells;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level, the substrate voltage regulator circuit comprising a series of diode connected transistors coupled between a supply voltage source and the substrate, and at least one bypass transistor coupled to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors,

each diode connected transistor of the series of diode connected transistors has a junction voltage drop, and the substrate voltage bias level is defined by a supply voltage level minus junction voltage drops of unbypassed diode connected transistors of the series of diode connected transistors.

38. (Previously Added) The DRAM of claim 37 wherein the substrate voltage regulator circuit includes a plurality of bypass transistors, each one of the plurality of bypass transistors coupled to at least one diode connected transistor in the series of diode connected transistors for electrically bypassing a plurality of diode connected transistors.

39. (Previously Added) The DRAM of claim 37 wherein the at least one bypass transistor is turned off during normal operation of the integrated circuit memory device such that the one diode connected transistor is unbypassed during normal operation but can be selectively bypassed during testing operations.

40. (Previously Added) The DRAM of claim 37 wherein the at least one bypass transistor is turned on during normal operation of the integrated circuit memory device such that the one diode connected transistor is bypassed during normal operation but can be selectively unbypassed during testing operations.

41. (Previously Added) A dynamic random access memory (DRAM), comprising:

an array of memory cells formed on a substrate;

a number of wordlines and a number of bitlines coupled to the array of memory cells;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level, the substrate voltage regulator circuit comprising a series of diode connected transistors coupled between a supply voltage source and the substrate, and a plurality of bypass transistors coupled to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors,

each diode connected transistor of the series of diode connected transistors has a junction voltage drop, and the substrate voltage bias level is defined by a supply voltage level minus junction voltage drops of unbypassed diode connected transistors of the series of diode connected transistors.

42. (Previously Added) The DRAM of claim 41 wherein the plurality of bypass transistors is turned off during normal operation of the integrated circuit memory device such that the one diode connected transistor is unbypassed during normal operation but can be selectively bypassed during testing operations.

43. (Previously Added) The DRAM of claim 41 wherein the plurality of bypass transistors is turned on during normal operation of the integrated circuit memory device such that the one diode connected transistor is bypassed during normal operation but can be selectively unbypassed during testing operations.